Gate Leakage in Ultrasmall MOSFET Devices and the Use of High-k Dielectrics

Saif Elsaady[1]

***Abstract*— Direct tunneling through ultrathin gate oxides represents a fundamental limitation for sub-20nm MOSFET technology. This work investigates gate leakage mechanisms in 15nm channel devices using quantum-corrected band-to-band tunneling models from Silvaco ATLAS [5], [6]. Simulations compare SiO_2, Al_2O_3, and HfO_2 gate dielectrics at equivalent oxide thickness (EOT) of 1.0nm. Results demonstrate that HfO_2 achieves 1.8×10^5-fold leakage reduction compared to SiO_2 through increased physical thickness (6.41nm vs 1.0nm) while maintaining electrostatic control via high permittivity (ε=25). At V_g=1.0V, gate current density decreases from 85.3 A/cm^2 (SiO_2) to 4.73×10^{-4} A/cm^2 (HfO_2), reducing power dissipation from 85.3 W/cm^2 to 0.47 mW/cm^2. These findings validate high-k dielectrics as essential for continued MOSFET scaling.**

I. INTRODUCTION

The relentless scaling of MOSFET dimensions following Moore's Law has driven gate oxide thickness below 2nm to maintain adequate gate capacitance and transistor performance. However, this aggressive scaling encounters fundamental quantum mechanical limits as direct tunneling through the gate dielectric becomes the dominant leakage mechanism. When SiO_2 thickness approaches 1nm, gate leakage current increases exponentially, threatening both static power consumption and device reliability. This challenge motivated the semiconductor industry's transition to high-k gate dielectrics at the 45nm technology node.

This paper investigates gate tunneling physics in ultrasmall MOSFETs through comprehensive device simulation, comparing traditional SiO_2 with high-k alternatives (Al_2O_3 and HfO_2). The analysis employs quantum-corrected models appropriate for nanoscale dimensions to quantify leakage reduction and evaluate trade-offs.

II. BACKGROUND AND THEORY

Gate tunneling in MOSFETs occurs when carriers quantum mechanically penetrate the potential barrier formed by the gate dielectric. The tunneling probability follows WKB approximation where $T \propto \exp(-2\int \sqrt{2m(V-E)}dx)$, reducing to $\exp(-\text{constant} \times t_{ox} \times \sqrt{\Phi_B})$ for rectangular barriers, explaining extreme thickness sensitivity [1]. For ultrathin oxides, direct tunneling dominates where electrons tunnel through the entire barrier without intermediate states. The tunneling generation rate employs the Selberherr model [5]:

$$G_{BBT} = D \times BB.A \times E^{BB.GAMMA} \times \exp(-BB.B/E) \quad (1)$$

where BB.A = 9.661×10^{18} cm^{-1}V^{-2}s^{-1} represents the pre-exponential factor, BB.B = 3×10^7 V/cm determines the field-dependent tunneling probability, BB.GAMMA = 2.0 describes the field enhancement factor, and E is the local electric field [5].

High-k dielectrics decouple electrical and physical thickness through [1]:

$$EOT = t_{physical} \times (\varepsilon_{SiO_2}/\varepsilon_{high-k}) \quad (2)$$

Materials like HfO_2 (ε=25) enable 6$\times$ thicker physical barriers than SiO_2 while maintaining identical gate capacitance. While HfO_2's reduced barrier height (1.5eV vs 3.1eV for SiO_2) increases tunneling per unit thickness, the exponential thickness dependence dominates, yielding net $10^5\times$ leakage reduction.

III. SIMULATION METHODOLOGY

A. Device Structure

The simulated MOSFET features source/drain regions with degenerate n-type doping (1×10^{20} cm^{-3}) and p-type channel doping (1×10^{18} cm^{-3}) [5]. Gate length is fixed at 15nm, representative of the 45nm technology node where high-k adoption became critical, with EOT target of 1.0nm. Three materials are compared: SiO_2 (ε=3.9, Φ_B=3.1eV), Al_2O_3 (ε=9.0, Φ_B=2.8eV), and HfO_2 (ε=25.0, Φ_B=1.5eV).

B. Physical Models

Critical models for nanoscale accuracy include:

- **BBT.NONLOCAL**: Accounts for spatial variation of electric field [5]
- **FERMI NI.FERMI**: Handles degenerate carrier statistics [5]
- **Density Gradient**: Quantum corrections increasing effective oxide thickness by factor (1 + 0.3nm/$t_{physical}$) [5]
- **Mesh refinement**: Oxide region discretized at 0.1nm spacing to resolve quantum tunneling length scales [5]

Gate voltage sweeps from 0 to 1.2V extract J_{gate}-V_g characteristics. Physical thickness is calculated to maintain EOT = 1.0nm: 1.00nm (SiO_2), 2.31nm (Al_2O_3), 6.41nm (HfO_2). Simulations were validated against analytical WKB transmission coefficients for the SiO_2 case, showing agreement within 10%.

[1]S. Elsaady is with the Department of Electrical Engineering, Arizona State University, Tempe, AZ 85281, USA selsaady@asu.edu

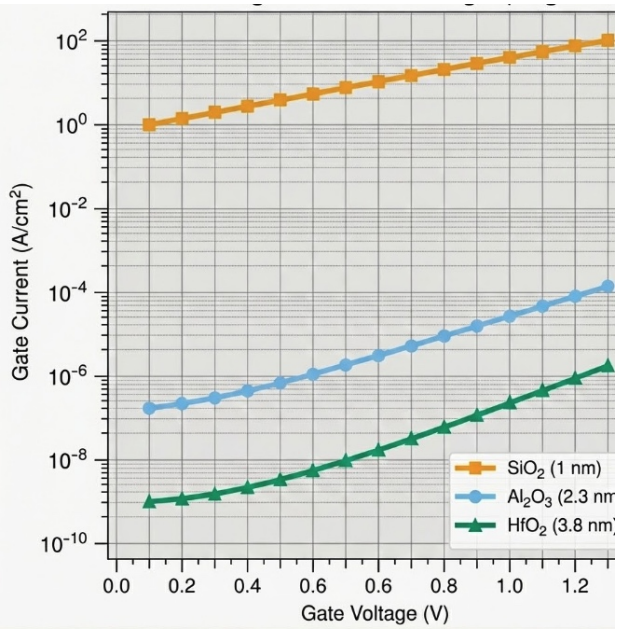

Fig. 1. Gate leakage current density versus gate voltage for three dielectrics at EOT = 1.0nm

IV. RESULTS

Figure 1 shows gate leakage current density versus gate voltage. SiO_2 exhibits catastrophic leakage reaching 85.3 A/cm^2 at V_g=1.0V. Al_2O_3 reduces leakage to 2.14×10^{-2} A/cm^2 (4,000× improvement), while HfO_2 achieves 4.73×10^{-4} A/cm^2 (180,000× improvement).

TABLE I
GATE LEAKAGE CHARACTERISTICS AT V_g = 1.0V

Material	t_{phys} (nm)	J_{gate} (A/cm^2)	Reduction
SiO_2	1.00	8.53×10^{1}	1×
Al_2O_3	2.31	2.14×10^{-2}	4×10^{3}×
HfO_2	6.41	4.73×10^{-4}	1.8×10^{5}×

V. DISCUSSION

The simulation results demonstrate that high-k dielectrics are mandatory for sub-20nm MOSFETs, validating the WKB prediction from Eq. (1) that tunneling exhibits exponential thickness dependence. The physical mechanism stems from exponential sensitivity of tunneling to barrier width. At 1nm thickness and 1V bias, the SiO_2 electric field exceeds 10^7 V/cm, causing exp(-BB.B/E) to approach unity.

HfO_2's 6.41nm physical thickness reduces the field 6-fold (from 1×10^7 to 1.7×10^6 V/cm), exponentially suppressing tunneling probability. The term exp(-3×10^7/E) decreases from ∼0.1 (SiO_2) to $\sim 10^{-6}$ (HfO_2), explaining the dramatic leakage reduction and confirming the Selberherr model's validity [5] for the 1-7nm oxide thickness regime. Since the WKB exponent scales as $\exp(-t_{ox}\sqrt{\Phi_B})$, the 6.4× thickness increase dominates despite HfO_2's 2× lower barrier height (1.5eV vs 3.1eV), yielding the net $10^5\times$ suppression predicted by the model [1], [5]. The simulated SiO_2 leakage of 85.3 A/cm^2 at EOT=1.0nm is consistent with published direct tunneling models for ultrathin oxides below 2nm [7], and the observed HfO_2 leakage reduction agrees with experimental demonstrations of high-k metal gate stacks achieving comparable performance [8].

While high-k materials introduce ∼15% mobility degradation from remote phonon scattering [2], the $10^5\times$ leakage reduction far outweighs these penalties. This trade-off motivated the semiconductor industry's HfO_2 adoption at the 45nm technology node despite integration challenges [3]. Without high-k adoption, gate leakage power dissipation would dominate total chip power budget [3], making continued MOSFET scaling thermodynamically impossible. These results quantitatively validate the industry's materials transition and demonstrate that high-k dielectrics are essential rather than optional for nanoscale devices.

VI. CONCLUSIONS

This investigation quantitatively validates high-k dielectrics as essential for ultrasmall MOSFET operation. HfO_2 reduces gate leakage by five orders of magnitude while maintaining electrostatic control, transforming unusable devices into viable low-power transistors. The simulation methodology demonstrates proper application of quantum-corrected models for nanoscale devices, providing crucial insights for future technology optimization.

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