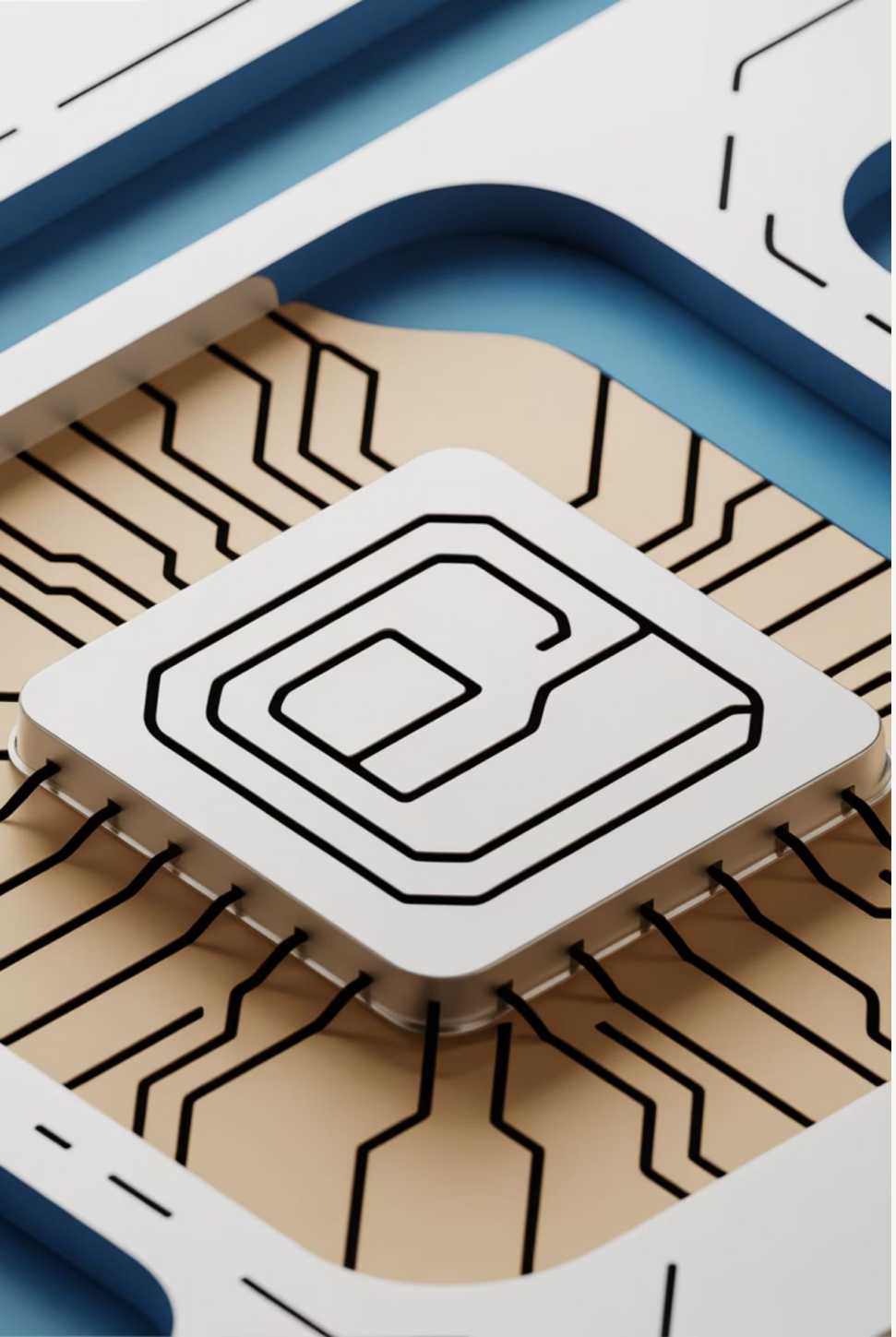

AI-Accelerated Signal Integrity in Chiplet-Based Semiconductor Packaging

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Academic & Industry Partners

- CHE 518 Course Instructors for comprehensive semiconductor packaging training. ***Dr. Terry Alford***
- Industry researchers advancing signal integrity methodologies
- UCIe Consortium for standardized chiplet interconnect specifications
- EDA tool developers: Cadence, Synopsys, Ansys, Siemens, Keysight

> *"Signal integrity analysis has been around for decades, but it takes on a whole new dimension in advanced packages"*

Motivation: The Chiplet Revolution & Signal Integrity Challenge

Why Chiplet Packaging?

Cost Efficiency

Nearly **50% cost reduction** vs monolithic advanced node designs

Superior Yield

Up to **97.3% yield** compared to 66.7% monolithic with same defect density

Modularity

Mix process nodes: advanced logic with older I/O and memory

Scalability

Overcome reticle limits of large monolithic dies

The Signal Integrity Challenge

Material Boundary Crossings

Multiple substrates, interposers, and layers create impedance mismatches

Longer Interconnects

Inter-die paths longer and less predictable than monolithic routing

Increased Crosstalk

Tightly packed traces amplify signal coupling effects

Complex Power Delivery

Multiple chiplets require careful noise mitigation strategies

Background: Chiplet Architectures & Signal Integrity Fundamentals

Chiplet Architecture Types

Modular Design

Separate functional blocks: CPU, GPU, memory, I/O into individual dies

2.5D Integration

Silicon interposers or organic substrates connect chiplets horizontally

3D Integration

Vertical stacking using TSVs and hybrid bonding for direct die-to-die connection

D2D Communication

Standardized interfaces: UCIe, MIPI for interoperability

Signal Integrity Fundamentals

Signal Quality

Correct timing, proper waveform shape, consistent voltage levels

Electromagnetic Modeling

At 16+ GT/s, full EM simulation required—not just RC extraction

RLC Analysis

Must account for resistance, inductance, capacitance including mutual effects

Complete Path Analysis

Model entire signal path from source through interposer to destination

Analog Nature of High-Speed

SerDes and high-speed interfaces require RF-level analysis

Signal Integrity Issues in Chiplet Packages

Frequency-Dependent Loss

Interconnects exhibit low-pass filter behavior. High-frequency components attenuate more than low-frequency, causing rise time degradation and reduced eye opening.

Crosstalk

Energy from adjacent aggressors couples into victim lines. Tight trace spacing exacerbates coupling, manifesting as noise peaks in eye diagrams.

Reflections

Impedance mismatches at die-interposer boundaries cause signal reflections. Multiple reflection points create standing waves on longer interconnects.

Interposer & TSV Effects

TSVs require RLC modeling at high frequencies. Vertical connections create additional discontinuities requiring specialized models.

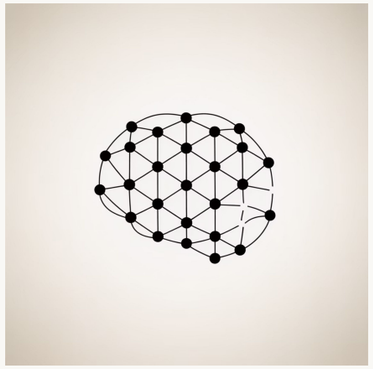
Process Variation Impact

Different chiplets from different fabs exhibit worse variation than monolithic. Substrate-induced skew adds timing uncertainty.

Complex Power Delivery

Decentralized power networks for multiple chiplets. Power noise couples into signal paths (SI-PI interaction). Ground bounce amplified.

Role of AI in Semiconductor Design & Packaging



AI/ML Applications

Machine Learning for SI Analysis

Train surrogate models on EM simulation data to predict VTF loss, crosstalk, eye diagrams without full EM solve

Predictive Modeling

Neural networks predict signal behavior from geometric parameters, reducing exhaustive simulation needs

Design of Experiments

Systematic exploration of multi-dimensional parameter space identifies critical design variables

Neural-Accelerated Simulation

Hybrid approach: ML predicts initial solution, EM refines for orders of magnitude speedup

Key Benefits

Reduced Iteration Cycles

ML predicts outcomes in seconds vs days. Enables exploration of thousands of design variants.

Improved Prediction Accuracy

ML models trained on validated EM data maintain fidelity, reducing silicon respins

Faster Time-to-Market

Accelerated design closure reduces overall development schedule

Enhanced Optimization

Multi-objective optimization: SI + PI + Thermal simultaneously

Proposed Workflow: AI-Accelerated Signal Integrity

Stage 1: Design Space Definition

- Define geometric parameters: trace width, spacing, length, stack-up
- Specify material properties: dielectric constant, loss tangent, conductivity
- Set interconnect parameters: bump pitch, TSV dimensions, channel topology
- Establish UCIe compliance requirements and manufacturing constraints

Stage 2: DOE-Based Intelligent Sampling

- Sample parameter space efficiently using DOE methodology
- Generate representative design variants covering critical regions
- Avoid exhaustive grid search (computationally prohibitive)
- Typical DOE: 100-1000 points vs millions in full factorial

Stage 3: ML Model Training & Validation

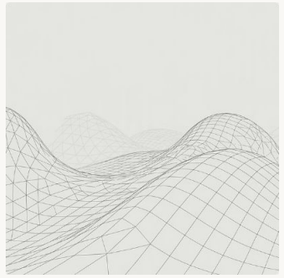
- Run full EM simulations on DOE sample points (baseline truth)
- Extract SI metrics: VTF loss, crosstalk, eye width/height, jitter
- Train ML surrogate models: neural networks, Gaussian processes
- Validate accuracy on hold-out test set until error < 5-10%

Stage 4: Rapid Optimization & SI Verification

- Use trained ML model for fast SI prediction across full design space
- Optimization algorithms guide design improvements
- Identify optimal configurations meeting UCIe specifications
- Final verification with targeted EM on optimized designs

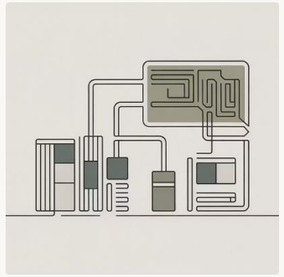
Modeling & Simulation Approach

Comparison of Simulation Methods



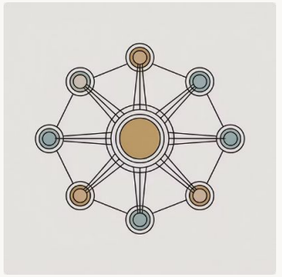
Full Electromagnetic Simulation

- **Accuracy:** Highest—solves Maxwell's equations
- **Capacity:** Thousands of signals
- **Time:** Hours to days
- **Best for:** Final verification, critical high-speed channels, TSV modeling



RC Extraction (Traditional)

- **Accuracy:** Lower fidelity—resistance and capacitance only
- **Capacity:** Millions to tens of millions of nets
- **Time:** Minutes to hours
- **Best for:** On-chip routing, lower-speed signals < 5 GHz
- **Limitation:** Misses inductance effects critical at high frequency



AI/ML Surrogate Models

- **Accuracy:** 90-95% of full EM (within 5-10% error)
- **Capacity:** Unlimited once trained
- **Time:** Seconds
- **Best for:** Design space exploration, optimization, early feasibility
- **Limitation:** Requires upfront training data, validity limited to training space

Recommended Hybrid Approach: Use ML for rapid exploration and optimization, apply full EM to validate final optimized designs. Iterate between fast ML and accurate EM for efficient workflow balancing speed and accuracy.

Design of Experiments for SI Parameter Space Exploration

Key Design Parameters

Geometric Parameters

Trace Width: 2-20 µm (affects impedance, current capacity)

Trace Spacing: Controls crosstalk coupling

Trace Length: Directly impacts loss and delay

Via & TSV Dimensions: Diameter, barrel length affect inductance

Interconnect Pitch

Bump Pitch: C4 spacing 100-150 µm

Micro-bump: 2.5D/3D typically 40-55 µm for UCIe

TSV Pitch: Vertical connection density in 3D stacks

Trade-off: Tighter = higher bandwidth but more SI challenges

Material Properties

Dielectric Constant (Dk): Affects propagation speed, impedance

Loss Tangent (Df): Determines dielectric loss at high frequency

Conductor Conductivity: Copper quality affects resistive loss

Interposer Material: Silicon (low loss) vs organic (lower cost)

DOE Methodology & Benefits

Sampling Strategies

Latin Hypercube: Efficient coverage of multi-dimensional space

Orthogonal Arrays: Minimize parameter correlation

Adaptive Sampling: Focus on regions of interest

Identify Critical Parameters

Statistical analysis reveals which variables matter most. Discover how parameters interact (e.g., narrow trace + tight spacing = severe crosstalk)

Optimize with Fewer Iterations

Directed improvement rather than random trial-and-error. Understand sensitivity and margins before committing to silicon

Statistical Analysis Outputs

Main effects plots, interaction plots, Pareto charts identify influential factors. Response surface models guide optimization

Case Study: AI-Based Optimization for UCIe Chiplet Channel

Scenario: 24 GT/s D2D Channel Design Challenge

DOE Sampling

50 design variants: vary trace width 6-12 µm, spacing 10-25 µm, layer assignment

EM Simulation

Full 3D EM on all 50 points. Extract VTF loss, crosstalk, eye diagrams. **100 hours compute time**

ML Training

Train neural network: [width, spacing, layer] → [VTF metrics, eye]. **94% validation accuracy**

Optimization

ML evaluates **10,000 candidates in 5 minutes**. Finds optimal: 9.5 µm width, 18 µm spacing

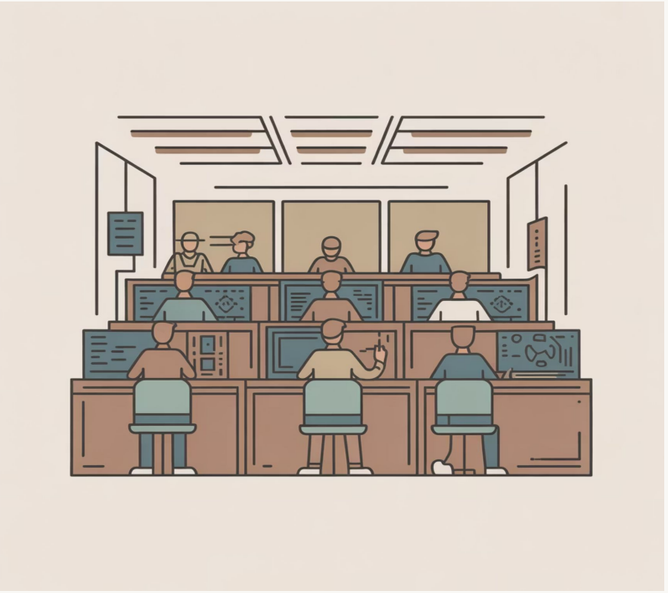
Equalization Tuning

ML predicts Tx de-emphasis: -3.5 dB, optimizes Rx CTLE settings per UCIe standard

Problem: Initial design fails UCIe VTF loss mask, shows crosstalk above 10 GHz, and lacks sufficient eye opening and timing margin.

Results:

- **Eye Height:** 48 mV vs 40 mV → **+20% margin**
- **Crosstalk: −40%**, comfortably below mask limit
- **Timing Margin:** 25 ps achieved vs 20 ps target → **+25%**
- **Design Speed: 50–100× faster** across **100+ channels**



Results & Discussion: Performance Gains

Computational Performance

ML achieves **100-1000x speedup** for individual evaluations and **50-200x** for complete package analysis

Accuracy Validation

ML Model Fidelity

Within 5-10% error vs full EM ground truth

VTF Loss Error

Typical prediction error ±0.5 dB over frequency range

Eye Metric Accuracy

Height/width predictions within ±5%

Design Quality Improvements

Yield Enhancement

5-10% improvement in usable design space through better SI margin allocation and process variation handling

SI Margin Gains

20-30% eye opening improvement. 48-52 mV achieved vs 40 mV baseline. Width margin: 10-15%

Timing Margin Enhancement

20-40% improvement through better skew and jitter control

Challenges & Limitations

Technical Challenges

1

Data Scarcity & Quality

Limited training data for novel designs. Each EM simulation expensive (hours). Need 100-1000+ samples. Cold-start problem for first-of-kind designs.

2

ML Generalization Limitations

Models only accurate **within training bounds.** Extrapolation unreliable. Must detect "out of distribution" designs. May miss physical phenomena not in training set.

Integration & Adoption Issues

1

Toolchain Integration

Must integrate with existing EDA flows (Cadence, Synopsys, Ansys). **Proprietary formats and APIs.** Workflow disruption and learning curve for designers.

2

Standardization Gaps

No standard format for ML models in EDA. UCIe provides electrical specs but not AI design guidelines. Interoperability challenges across vendors.

Future Work & Research Directions

On-Device LLMs

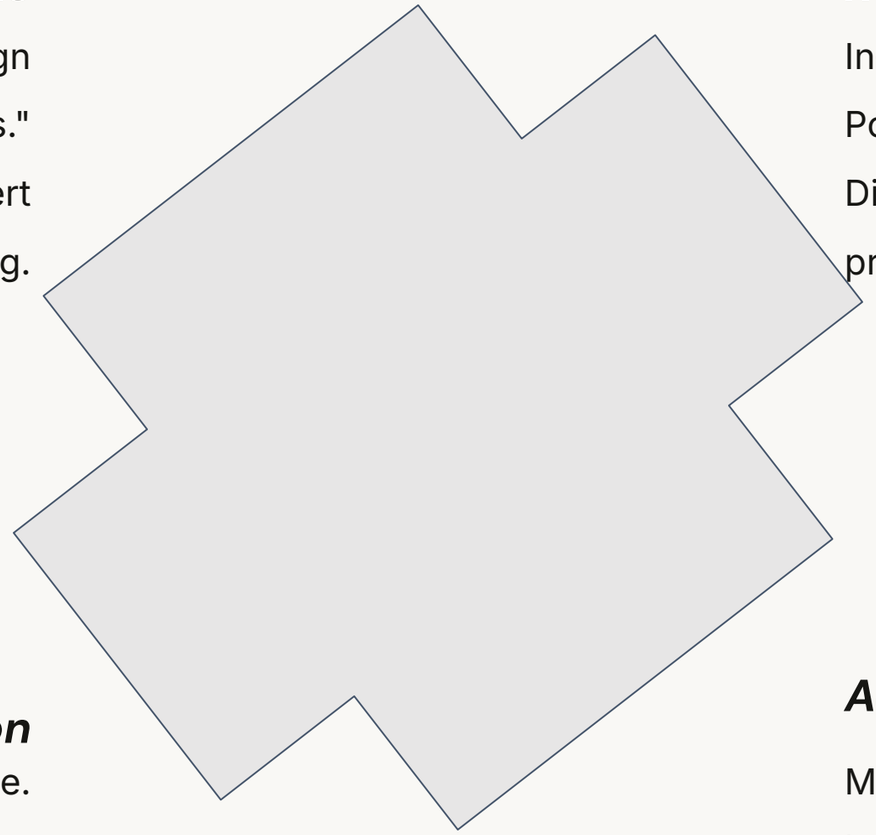
Natural language design interfaces: "Design UCIe channel for 32 GT/s < 2 dB loss." Automated documentation and expert system for SI troubleshooting.

Automated Design Rules

ML-derived rules from successful designs. Adapt rules to new process nodes automatically. Constraint optimization for yield.

Reliability & Aging Prediction

ML predicts SI degradation over lifetime. Electromigration, stress-induced voiding effects. Design for 10-year reliability.



Real-Time SI Monitoring

In-situ measurement during fabrication. Post-silicon validation closes the loop. Digital twin concepts for reliability prediction.

SI-PI-Thermal Co-Optimization

Simultaneous multi-physics optimization. ML models predict all three domains. Pareto-optimal designs balancing objectives.

Advanced Materials & Processes

ML predicts SI for novel dielectrics. Optical interconnects, wireless die-to-die. Hybrid bonding with 1-2 µm pitch.

Impact & Implications

Industry Impact

Commercial Chiplet Ecosystem

AI tools ensure **UCIe compliance,** reduce multi-vendor integration risk. Enable true plug-and-play chiplet interoperability.

Economic Benefits

20-40% reduction in package design expenses. 2-4 month schedule reduction. 5-10% yield improvement potential.

Competitive Advantage

Companies with AI-driven capabilities deliver **better products faster.** Enable push to 32+ GT/s data rates.

Broader Industry Transformation

Democratization of advanced packaging. AI tools make complex designs accessible to smaller companies.

Academic & Educational Impact

Research Opportunities

Novel ML architectures for physical design. Physics-informed neural networks. Multi-disciplinary collaboration across departments.

Curriculum Development

Update coursework with **AI-driven methodologies.** Train students in both SI fundamentals AND ML techniques.

Teaching & Mentoring

AI tools **lower barrier to entry** for underrepresented groups. Visual, data-driven approaches complement traditional theory.

Broader Societal Impact

Advanced packaging enables **affordable high-performance computing.** Benefits AI, healthcare, climate modeling, education.

Open Science & Collaboration

Community repositories for training data. **Open-source ML models.** Accelerate innovation through collaboration.

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> "The best way to solve any signal integrity problem is to find the root cause"